What is claimed is:

1. A magnetic memory device comprising:

a semiconductor substrate;

a transistor formed above said semiconductor substrate;

a tunnel magneto-resistive element formed above an interlayer dielectric film covering said transistor of said semiconductor substrate;

a first wiring line buried in said interlayer dielectric film and connected to a source/drain diffusion layer of said transistor;

a second wiring line buried under said tunnel magneto-resistive element while overlying said first wiring line in said interlayer dielectric film, to provide a current magnetic field to said tunnel magneto-resistive element during writing; and

a third wiring line connected to an upper surface of said tunnel magneto-resistive element and provided to cross said second wiring line, to provide a current magnetic field to said tunnel magneto-resistive element during writing and also to cause a cell current to flow during reading,

wherein said second wiring line is formed and patterned so that its both edges are placed outside the pattern of said tunnel magneto-resistive element.

2. The device according to claim 1, wherein said first wiring line is formed by patterning so that its both edges are placed outside of the pattern of said tunnel magneto-resistive element.

3. The device according to claim 2, wherein a gate wiring line of said transistor is patterned to pass through a region immediately beneath said tunnel magneto-resistive element while having a width greater than that of said tunnel magneto-resistive element.

4. The device according to claim 2, wherein a gate wiring line of said transistor is patterned to extend outside of a region immediately beneath said tunnel magneto-resistive element.

5. The device according to claim 2, wherein the first and second wiring lines are formed by patterning to pass through a region immediately beneath said tunnel magneto-resistive element while having a width greater than that of said tunnel magneto-resistive element.

6. The device according to claim 3, wherein a gate wiring line of said transistor is patterned to pass through a region immediately beneath said tunnel magneto-resistive element while having a width greater than that of said tunnel magneto-resistive element.

7. The device according to claim 3, wherein a gate wiring line of said transistor is patterned to extend outside of a region immediately beneath said tunnel magneto-resistive element.

8. A magnetic memory device comprising:

a semiconductor substrate;

a transistor formed above said semiconductor substrate;

a tunnel magneto-resistive element formed above an interlayer dielectric film covering said transistor of said semiconductor substrate;

a first wiring line buried in said interlayer dielectric film and connected to a source/drain diffusion layer of said transistor;

a second wiring line buried under said tunnel magneto-resistive element while overlying said first wiring line in said interlayer dielectric film, to provide a current magnetic field to said tunnel magneto-resistive element during writing; and

a third wiring line connected to an upper surface of said tunnel magneto-resistive element and provided to cross said second wiring line, to provide a current magnetic field to said tunnel magneto-resistive element during writing and to cause a cell current to flow during reading, wherein

all of element regions including all wiring lines including the first and second wiring lines formed under said tunnel magneto-resistive element above said semiconductor substrate, a gate wiring line of said transistor, more than one wiring contact and the source/drain diffusion layer are formed by patterning so that edges thereof are placed outside of a region immediately underlying said tunnel magneto-resistive element.